

**S/N Unknown**

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Kie Y. Ahn et al.

Examiner: Unknown

Serial No.: Unknown

Group Art Unit: Unknown

Filed: Herewith

Docket: 303.678US4

Title: STRUCTURE AND METHOD FOR DUAL GATE OXIDE THICKNESSES

**PRELIMINARY AMENDMENT**

BOX PATENT APPLICATION

Commissioner for Patents

Washington, D.C. 20231

Sir:

Prior to taking up the above-identified patent application for examination, please amend the application as follows:

**IN THE SPECIFICATION**

On page 1, line 3, before the heading, "Field of the Invention", insert the following paragraph:

**Cross Reference to Related Application(s)**

This application is a division of U.S. Patent Application No. 09/514,629, filed on February 28, 2000, the specification of which is incorporated herein by reference.

**IN THE CLAIMS**

Please cancel claims 1 - 40, without prejudice or disclaimer, after adding the following new claims.

55. (New) A circuit on a single substrate, comprising:

a logic device, wherein the logic device includes a transistor with a dielectric layer including:

a first dielectric layer of a first thickness less than 5 nanometers;

a top layer which exhibits a high resistance to oxidation at high temperatures; and

a memory device coupled to the logic device, wherein the memory device further includes a transistor with a second dielectric layer having a second thickness greater than the dielectric layer of the first thickness.

56. (New) The circuit of claim 55, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

57. (New) The circuit of claim 55, wherein first dielectric layer of a first thickness includes silicon dioxide ( $\text{SiO}_2$ ) and the top layer includes silicon nitride ( $\text{Si}_3\text{N}_4$ ).

58. (New) The circuit of claim 55, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide ( $\text{SiO}_2$ ).

59. (New) The circuit of claim 55, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

60. (New) The circuit of claim 55, wherein the top layer includes a top layer of silicon nitride ( $\text{Si}_3\text{N}_4$ ) which comprises approximately a third of the first thickness of the first dielectric layer.

61. (New) The circuit of claim 55, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

62. (New) A circuit on a single substrate, comprising:

a logic device, wherein the logic device includes a transistor with a dielectric layer including:

a first dielectric layer of a first thickness less than 5 nanometers;

a top layer which exhibits a high resistance to boron penetration at high temperatures; and

a memory device coupled to the logic device, wherein the memory device further includes a transistor with a second dielectric layer having a second thickness greater than the dielectric layer of the first thickness.

63. (New) The circuit of claim 62, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

64. (New) The circuit of claim 62, wherein first dielectric layer of a first thickness includes silicon dioxide ( $\text{SiO}_2$ ) and the top layer includes silicon nitride ( $\text{Si}_3\text{N}_4$ ).

65. (New) The circuit of claim 62, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide ( $\text{SiO}_2$ ).

66. (New) The circuit of claim 62, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

67. (New) A circuit on a single substrate, comprising:

a logic device, wherein the logic device includes a transistor with a dielectric layer including:

a first dielectric layer of a first thickness less than 5 nanometers;

a silicon nitride ( $\text{Si}_3\text{N}_4$ ) top layer which exhibits a high resistance to oxidation at high temperatures; and

a memory device coupled to the logic device, wherein the memory device further includes a transistor with a second dielectric layer having a second thickness greater than the dielectric layer of the first thickness.

68. (New) The circuit of claim 67, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

69. (New) The circuit of claim 67, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide ( $\text{SiO}_2$ ).

70. (New) The circuit of claim 67, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

71. (New) The circuit of claim 67, wherein the silicon nitride ( $\text{Si}_3\text{N}_4$ ) top layer includes a silicon nitride ( $\text{Si}_3\text{N}_4$ ) top layer with a thickness of approximately a third of the first thickness of the first dielectric layer.

72. (New) The circuit of claim 67, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

73. (New) A circuit on a single substrate, comprising:

a logic device, wherein the logic device includes a transistor with a dielectric layer including:

a first dielectric layer of a first thickness less than 5 nanometers;

a silicon nitride ( $\text{Si}_3\text{N}_4$ ) top layer of approximately a third of the first thickness which exhibits a high resistance to oxidation at high temperatures; and

a memory device coupled to the logic device, wherein the memory device further includes a transistor with a second dielectric layer having a second thickness of less than 12 nanometers (nm).

74. (New) The structure of claim 73, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

75. (New) The structure of claim 73, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

76. (New) The structure of claim 73, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide ( $\text{SiO}_2$ ).

77. (New) A circuit on a single substrate formed by the method comprising:
- forming a logic device including a first transistor and a memory device including a second transistor on a single substrate;
  - forming a pair of gate oxides on the first transistor and the second transistor to a first thickness of less than 5 nanometers (nm) by krypton plasma generated atomic oxygen at approximately 400 degrees Celsius;
  - forming a thin dielectric layer on one of the pair of gate oxides, wherein the thin dielectric layer exhibits resistance to oxidation at high temperatures; and
  - forming the other of the pair of gate oxides to a second thickness.

[illegible]

**PRELIMINARY AMENDMENT**

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Page 6

Dkt: 303.678US4

**REMARKS**

Claims 1 - 40 are canceled without prejudice or disclaimer and claims 55 - 77 were added. Claims 41 - 77 are now pending in this application.

The specification is amended to add a cross reference to the prior application. No new matter is added by way of these amendments.

The application filing fee as calculated on the application transmittal sheet reflects the amendments to the claims described above.

The Applicant respectfully requests that the preliminary amendment described herein be entered into the record prior to examination and consideration of the above-identified application.

Respectfully submitted,

KIE Y. AHN ET AL.

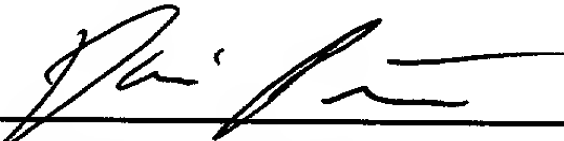
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